AGC
Your Dreams, Our Challenge

EZ-IO-F

General Processing Guidelines

General Information

EZ-IO-F laminates are thermally stable, nanoparticle ceramic-filled, PTFE materials. They were developed to meet the demanding requirements for thermally stable dielectric constants and plated through-hole reliability in extreme environmental conditions.

AGC's ceramic/PTFE laminates are low loss, dimensionally stable, thin core materials for multilayer digital or RF applications that can be combined with our fastRise prepregs for the lowest stripline insertion losses. A lightweight style of fiberglass and very high loadings of ceramic particles yield excellent dimensional and electronic performance, as well as ease of processing.

Storage

EZ-IO-F laminates should be stored flat in a clean dry area at room temperature. Cores will benefit from being stored between two stiffeners in order to prevent unnecessary bending of the layers or damaged corners. Soft slip sheets should be used to prevent dust and debris from being embossed into the material. With proper storage conditions, cores have an indefinite shelf life.

Handling

PTFE is a thermoplastic material which is very stable electrically and chemically when compared with common thermosetting resins such as epoxy, polyphenyleneoxide, polyimide and cyanate ester. Part of what gives PTFE its superior performance over frequency and temperature also makes the pure resin relatively soft.

It is for this reason that most AGC laminates are reinforced with glass fabric. The glass fabric reinforcement of the substrate greatly increases stability in the X and Y axis over non-woven or unreinforced PTFE products. While the glass fabric provides excellent dimensional stability, the following process and handling precautions should be taken to prevent damage or deformation of the laminate during fabrication.

Avoid mechanical scrubbing

As with thin core or flexible substrates, mechanically scrubbing will stretch and deform the material. The pinch rollers used to secure the panel during scrubbing will also cause dents as particle or brush material are pressed into the surface of the laminate.

Chemical cleaning is preferred. Eliminating mechanical cleaning and unnecessary handling will improve the dimensional accuracy of subsequent processes by preventing mechanical distortion of the laminate.

Do not pick up a panel by one edge

Allowing the material to "flop" may stretch the copper and substrate. Lift the panel by two parallel edges; preferably the two closest dimensionally.

Do not stack panels directly on top of each other

The weight of the panels may emboss any particles or debris on the surface of the panel into adjacent panels. If panels must be stacked, use clean soft slip sheet material between each panel and keep stack height to a minimum. Prevent contaminant deposits on the material or copper.

The use of clean protective gloves and slip sheets will prevent contamination and staining. Keep work surfaces clean, dry, and completely free of debris.

Innerlayer preparation for multilayer

Multilayer applications require that two or more laminates be bonded together to form a single circuit board. There are two important considerations when processing the circuit board. The first is registration of the features from one layer to another. The second is the condition of the bond surface prior to lamination.

Acclimation

If the laminates has been extreme temperatures during shipment or storage, the material should be placed in ambient conditions for 24 hours prior to processing. If exposed to high humidity over 50%RH, proper baking process prior to fabricating PCB process is necessary.

Scaling

This data is for reference only and is dependent on numerous factors such as laminate thickness, copper thickness, copper types, circuit design, adjacent laminates / prepregs, lamination parameters, etc. Most PCB fabricators determine artwork compensation data by running a pilot lot or estimating based on previous experience.

In general, registration of layers can be improved by retaining as much copper as possible.

	Dimensional Change in Parts Per Million (PPM)	
	Machine Direction	**Cross Direction**
EZ-IO-F (≥0.010" core)	400-600	200-400
EZ-IO-F (0.005" core)	600-800	400-600

Surface preparation

A chemical process consisting of organic cleaners and a micro etch is the preferred method of preparing copper surfaces for coating with photoresist. Mechanical scrubbing is not recommended due to the distorting the thin laminate or imparting deep scratches that change the functional spacing. Both liquid and dry film photoresist can be applied.

EZ-IO-F laminates are compatible with most oxide and oxide alternative processes. Highly caustic, high temperature processes, such as traditional or reduced black oxides, should be followed by a thorough rinse and bake of the inner layers.

Special pretreatments of etched surfaces using sodium or plasma processes are not generally needed if care was taken to protect the substrate surface after copper etching. Removal of volatile substances prior to MLB bonding should be ensured by proper baking process at 110~125 ℃ for 0.5~2 hours.

Multilayer

For best results, EZ-IO-F laminates should be bonded using low loss bond ply such as fastRise™ series provided by AGC. The press cycle can be determined by the requirements of the chosen adhesive system of bondply and EZ-IO-F laminates are compatible with most adhesive systems. Please refer to AGC process guidelines for fastRise.

Drilling

Drill bits

Standard 130°-point geometry, 32□ - 45□ helix angle PCB carbide drills work well with EZ-IO-F laminates. Stack height should not exceed 2/3 the flute length of the smallest diameter drill being used.

Sharp drill bits are critical to any PTFE drilling; new drill bits should always be used. Undercut drill bits are recommended, but past studies have shown that some drill bit brands may obtain better results using their standard drill bits.

Chip Load

A nominal chip load of 0.001" (25 µm) is a recommended starting point for all tool sizes. Some fabricators find their combination of machines and tools allow for optimal chip loads as high as 0.002" (50 µm). For bit sizes under 0.010", decreasing the chip load incrementally from 0.001" (25 µm) has been found to offer some quality improvements. Fabricators should experiment within this range of chip loads until an optimal balance can be found between clean cut hole walls and drill smear.

If drill smear is visible and bits are sharp, reduce chip load until it is eliminated.

Cutting speed

Drill speeds of 100 SFM (30.5 m/min) or less is recommended. Slower speeds offer the greatest hole quality improvements. They allow generated heat to dissipate before smearing PTFE. Drill speed can be increased due to equipment limitations but added dwell times may become important. At a simple application, surface speeds of 300 SFM (90 m/min) could also provide acceptable hole quality.

Dwell Time

Drill speeds of 100 SFM (30 m/min) are recommended. Slower speeds offer the greatest hole-quality improvements; they allow generated heat to dissipate before smearing PTFE. In certain stack ups, drill speed can be increased to 150-200 SFM (45-60 m/min) to improve productivity without sacrificing quality but added dwell times may become more important.

If drill smear is visible and bits are sharp, reduce cutting speed until it is eliminated.

Peck Drilling

Peck drilling should be avoided where possible; it has been shown to increase drill bit wear as well as increase process time. Peck drilling may be required in some situations (e.g. bird nesting, hole plugging, chip extraction on thick panels, breaking thin drill bits, etc.). Peck drilling with a full withdrawal of the drill bit after each peck will reduce heat buildup and debris accrual. A general rule of thumb for peck depth is 20 to 30 mils per peck and should be optimized at the board shop.

If traditional peck drilling is not used, hole-wall quality may be improved with the use of a "clean" peck where the peck depth is set to equal that of the Phenolic entry. In this, the entry material will effectively clean the drill bit, retract to clear Phenolic debris and cool, and then reenter to drill the hole.

If tool breakage is an issue for small diameter, high aspect ratio holes, peck drilling may be inevitable. However, for 0.020" holes with an aspect ratio of roughly 12:1 or less, it is not clear that peck drilling is required. Some drill studies suggest that peck drilling will leave a small circular ring where the drill bits stop in the hole.

Hit Count

EZ-IO-F has been engineered to extend tool life in drill. The nanoparticle ceramic tends to be evacuated from the hole without abrading the actual edge of the drill bit. Hit counts of 700-1,000 hits per bit can be attained with the proper drill parameters. Hit count should always be baselined with a cross sectional analysis to determine when hole quality begins to degrade.

Entry / backup materials

Standard phenolic (0.024" thickness) and aluminum (0.007"- 0.015") entry material is recommended. Thicker phenolic (0.048" +) may be necessary on panels thicker than 0.200". A phenolic backup board (from 0.040" to 0.125" thickness) such as LCOA Spectrum Gold is recommended to reduce bottom-side burring and drill smear. Recent data suggest the harder materials will better clean the bits and prevent drill smear if other changes to drill parameters are not effective. It is critical to fully plunge the drill bit into the phenolic backup to clean off debris before retracting the bit through the PCB and potentially re-depositing it on the hole wall. The addition of lubricated backups, such as Slickback, are optional but do provide some marginal effectiveness at reducing heat buildup on the drill bit, which ultimately leads to drill smear.

Aluminum and phenolic serve to abrade PTFE debris off the bit. Optimizing the amount of phenolic to clean the drill tool between hits prevents bird nesting and smear and is a necessary factor in high quality EZ-IO-F drilled holes. Do not worry about phenolic causing excessive drill wear. Although the process window is wider for drilling double sided PCBs vs. multilayer PCBs, one should follow the same strategies and tactics that one would use to fabricate a multilayer based on EZ-IO-F cores.

The pressure of the drill foot should be a minimum of 40 psi and should be increased if topside burring is excessive.

Quick start

The following chart is provided as a general starting point for drill process development. The user shall determine the optimized conditions and suitability.

	Units
Entry Material	Phenolic (0.010"-0.024"/ 0.25-0.6 mm)
Backer Material	Rigid Phenolic, Slickback, or comparable
Cutting Speed	100 - 200 SFM (30.5 - 91.5 m/min)
Chip Load	0.0010 - 0.0015 in (25.4 - 38.1 µm)
Dwell	0 - 1000 ms
Hit Count	700 - 1000

Drill charts

Following table can be used as general starting point of recommended drilling parameters;

Diameter (in)	Spindle Speed (krpm)	Infeed (IPM)	Retract (IPM)	Remark
0.0079	70	70	300	
0.0100	67	70	400	
0.0140	55	65	500	
0.0200	46	58	500	
0.0280	34	46	500	
0.0310	30	42	500	
0.0400	24	35	500	
0.0490	20	30	500	
0.0590	20	30	500	
0.0980	20	30	500	

PLATING

EZ-IO-F laminates have been engineered to be highly resistant to chemical infiltration and a robust hole wall preparation process is necessary for a successful deposition plating process. Following hole wall preparation, EZ-IO-F will accept standard electroless copper or direct deposit metallization plating process. For high aspect radios or other difficult to plate applications, a second pass through the electroless process may be required to ensure proper hole-wall coverage. It may also be beneficial to run a short duration of electrolyzed copper, rinse etc. then restart the electrolyzed copper from the beginning to expose the hole wall to fresh chemistry.

IMAGE, DEVELOP, ETCH, STRIP

When copper surface preparation is required, chemical cleaning processes are preferred (e.g. microetch); Mechanical scrubbing (e.g. pumice scrub) should be avoided due to possible mechanical damage. Otherwise, standard processing should be used.

SOLDER MASK

No special treatment is required if the surface has not been mechanically scrubbed. In rare cases, where adhesion is poor, a plasma treatment may be used to activate the exposed PTFE.

ROUTING / MILLING

PCBs using EZ-IO-F can be successfully machined using standard router bits or end mills. Rigid phenolic entry and a rigid backer should be used. In some cases, adding paper (white paper or Kraft paper) between the phenolic and the part allows better conformance to surface topography (e.g. circuits, solder mask, etc.) and may reduce burring. For tight tolerances or superior edge quality, a "rough cut" placed 0.005 in. -0.010 in. (0.13 – 0.25 mm) off the part edge may be run prior to the "finish" cut at the nominal part edge. Metallic bits for PTFE board fabrication are recommend. EZ-IO-F materials will generally provide a better edge quality than is possible with the glass reinforced materials.

Following table can be used as general starting point of recommended routing parameters;

Router Diameter		Spindle Speed		Feed Rate
(mils)	(mm)	(kRPM)	(in/min)	(m/min)
33	0.8	50	10.8	0.27
39	1.0	40	12.2	0.31
47	1.2	34	12.6	0.32
63	1.6	25	18.7	0.48
78	2.0	20	27.2	0.69
94	2.4	20	35.0	0.89
118	3.0	20	42.5	1.08
125	3.2	20	43.3	1.10

Hole wall preparation

The debris loosely deposited in the holes can be removed by using a vapor or hydro-honing process. These processes involve directing water suspended abrasive particles through drilled holes. Due to the softness, EZ-IO-F laminates should be properly supported through these processes.

Desmear

Plasma

If panels have been exposed to moisture, bake the boards at 110 ºC for 1 hour. PTFE composites are usually not desmeared but the adhesive system used to bond multilayer require desmear. Standard FR4/epoxy desmear processes should then be used. The desmear plasma time is typically half of that of standard FR4/epoxy times because fastRise resin system tends to etch back very quickly.

Permanganate

Permanganate desmear is not recommended and has been shown to be very aggressive on fastRise resulting in excessive etchback. This is due to the high silica filler content and thermoset content in the resin system. Neither process (Plasma and Permanganate) will have a significant effect on EZ-IO-F materials but should be done prior to activation of PTFE (EZ-IO-F) surface.

PTFE Activation

Plasma

If panels have been exposed to moisture, bake the boards at 110 ºC for 1 hour. Plasma treat the PTFE resin using 70%/30% hydrogen/nitrogen gas mixture. 100% helium may also suffice. Power settings for the RF-signal generator are typically 60~75 % of full rated power for 30~60 minutes. Thick panels or high-aspect ratio holes may require extended plasma cycle times. Thick panels may also benefit from an additional 30miutes O2 plasma process prior to the PTFE activation plasma.

Sodium Etch

Sodium Etches (e.g. Fluoroetch) work well. Follow the manufacturer's recommended treatment process. Subsequently, bake for 1 hour at 120 ºC prior to plating to remove moisture that may have been absorbed during the sodium treatment process. Chlorine can have adverse effects on the sodium treatment. Do not subject exposed sodium etch treated holes to heavily concentrated chlorine-based chemical processes.

Process Example

The following table is offered by March Plasma as a basic starting point recipe;

Power(kW)	Pressure(mT)	Gasses	Gas Ratios	Flow(slm)	Pnl Temp (ºC)	Time(min)	Function
4.5	250	O_2 / N_2	90 / 10	2.5	90	A/R	Heating
4	250	CF_4 / O_2	10 / 90	2.5	99	10	Thermoset etch-back
4	250	O_2	100	2.5	99	5	Removes fluorine and cleans others
4.2	250	N_2	100	2.5	99	30	Activate PTFE. H2/N2 Cycle is typically more effective and reliable.

These guidelines can provide only basic and reference information for PCB fabricators. Because of different environment, equipment, tooling and so on, in all instances, the user shall determine suitability in any given conditions or applications. For more detailed processing information, please contact with the AGC engineer or sales representative.